



PATENT

#15  
C.B.  
2/26/04

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: )

Jeffrey S. Mailloux et al. )

Serial No.: 08/650,719 )

Filed: May 20, 1996 )

For: ASYNCHRONOUSLY- )

ACCESSIBLE MEMORY )

DEVICE WITH MODE )

SELECTION CIRCUITRY )

FOR BURST OR )

PIPELINED OPERATION )

Examiner: Hong C. Kim

Group Art Unit: 2186

Docket: 303.623US1

RECEIVED

JAN 21 2004

Technology Center 2100

APPELLANTS' BRIEF ON APPEAL

Mail Stop AF  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

This Appeal Brief is presented in support of the Notice of Appeal to the Board of Patent Appeals and Interferences, filed on November 13, 2003, from the Final Rejection of claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64 of the above-identified application, as set forth in the Final Office Action mailed on May 13, 2003.

This Appeal Brief is filed in triplicate. The Commissioner of Patents and Trademarks is hereby authorized to charge Deposit Account No. 19-0743 in the amount of \$330.00 which represents the requisite fee set forth in 37 C.F.R. § 117(c). The Appellants respectfully request consideration and reversal of the Examiner's rejections of pending claims.

01/20/2004 3DIRETAI 00000024 08650719

01 FC:1402

330.00 DP



RECEIVED

JAN 21 2004

Technology Center 2100

APPELLANTS' BRIEF ON APPEAL

TABLE OF CONTENTS

	<u>Page</u>
1. REAL PARTY IN INTEREST .....	1
2. RELATED APPEALS AND <del>INTERFERENCES</del> .....	1
3. STATUS OF THE CLAIMS .....	1
4. STATUS OF AMENDMENTS .....	1
5. SUMMARY OF THE INVENTION .....	2
6. ISSUES PRESENTED FOR REVIEW .....	2
7. GROUPING OF CLAIMS .....	3
8. ARGUMENT .....	3
a) The Applicable Law .....	3
b) The Reference .....	4
c) Discussion of the Rejections .....	4
c.1 -- The rejection under § 112 .....	4
c.2 -- The rejection under § 102 .....	5
c.2.1. <i>Why the reference does not disclose each and every element of the claimed subject matter as arranged in the claims</i> .....	6
c.2.2. <i>Why the reference does not disclose the claimed subject matter in as complete detail as is contained in the claim</i> .....	7
c.3 -- Why the claims are separately patentable .....	11
c.4 -- The double patenting rejection .....	14
9. SUMMARY .....	15
APPENDIX I	
The Claims on Appeal .....	16
APPENDIX II	
Reference .....	21



## **REAL PARTY IN INTEREST**

The real party in interest of the above-captioned patent application is the Assignee, Micron Technology, Inc.

## **2. RELATED APPEALS AND INTERFERENCES**

There are no interferences known to Appellants, Appellants' legal representative, or the Assignee that will directly affect or be directly affected by or have a bearing on the Board's decision in the appeal in this matter.

There are four appeals known to Appellants, Appellants' legal representative, or the assignee that may directly affect or be directly affected by or have a bearing on the Board's decision in the appeal in this matter. These related appeals are currently pending before the Board and concern U.S. Patent Application Serial Number 08/984,560 (Atty. Ref. No. 303.623US2), U.S. Patent Application Serial Number 08/984,562 (Atty. Ref. No. 303.623US3), U.S. Patent Application Serial Number 08/984,563 (Atty. Ref. No. 303.623US4), and U.S. Patent Application Serial Number 08/984,701 (Atty. Ref. No. 303.623US5). A fourth, related appeal was also pending with respect to U.S. Patent Application Serial Number 08/984,561 (Atty. Ref. No. 303.623US6). However, a Notice of Allowability indicating allowance of all claims has been mailed to the Appellants (Paper 32), and this matter is no longer before the Board.

## **3. STATUS OF THE CLAIMS**

Claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64 are currently pending, and the rejection of these claims is appealed. A list of the pending claims is included as Appendix I.

## **4. STATUS OF AMENDMENTS**

No amendments have been made subsequent to the Supplemental Response to the Second Final Office Action mailed to the Appellants on March 15, 2002, in which claim 7 was amended to correct a typographical error.

## **5. SUMMARY OF THE INVENTION**

As described in the Appellants' specification at page 7, line 6 - page 8, line 13, and shown generally in figures 9-11, the embodiments disclosed relate to a memory device that selectably operates using both burst and pipelined modes of operation. In one embodiment, an asynchronously addressable storage device 100 (shown in FIG. 9) includes mode circuitry 121 configured to select between burst and pipelined modes, and circuitry 122 operable in either the burst mode or pipelined mode and configured to switch between the burst mode and the pipelined mode for operating the device 100 in either mode. (Pg. 29, lines 5-25). Some embodiments can switch between burst access and ... pipelined modes of operation without ceasing ("on the fly"). (Pg. 33, lines 17-19). In the burst mode of operation, an externally-generated memory address stored in the circuitry 122 is first used to select data within the device 100. A counter 149 included in the circuitry 122 then increments the stored external address to internally generate addresses for subsequent accesses. In the pipelined mode of operation, the circuitry 122 uses external addresses 115 to access data within the device 100. (Pg. 29, lines 8-16). As address information passes through the memory, it is operative in one operational area before moving into another operational area. However, once moved, another set of address information may enter the operational area exited, and accesses to memory may overlap without conflicting. (Pg. 8, lines 1-5). In addition to the embodiments described herein, other embodiments of varying scope, such as systems, methods, and storage devices, including memory circuits, are disclosed. (Pg. 33, line 23 - Pg. 40, line 19).

## **6. ISSUES PRESENTED FOR REVIEW**

- 1) Whether claim 61 was properly rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.
- 2) Whether claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64 were properly rejected under 35 USC § 102(e) as being anticipated by U.S. Patent No. 5,610,864, issued to Manning (hereinafter "Manning").

## **7. GROUPING OF CLAIMS**

All claims are to be taken independent of each other and each stands alone for purposes of this Appeal.

## **8. ARGUMENT**

### ***a) The Applicable Law***

To make out a *prima facie* case of lack of written description under the first paragraph of 35 U.S.C. § 112, four elements must be shown:

- 1) The application does not reasonably describe or convey the concepts
- 2) to one of ordinary skill in the art
- 3) at the time of filing the patent application
- 4) of the claimed invention.

It is respectfully noted that “[i]f even one of these elements of the *prima facie* case is not present, the rejection is improper and must be withdrawn.” *See* Patent Prosecution: Practice and Procedure Before the U.S. Patent Office by Irah H. Donner, pg. 738, 2002. Since “[t]he initial burden is on the PTO to establish that the now claimed subject matter is not described by the specification ...”, the Office must show why this element is not sufficiently described in the application as to each element of the *prima facie* case. *Id.*, citing *Ex parte Anderson*, 21 U.S.P.Q. 2d 1241 (B.P.A.I. 1991).

Establishing anticipation under 35 U.S.C. § 102 requires the disclosure in a single prior art reference of each element of the claim under consideration. *In re Dillon* 919 F.2d 688, 16 USPQ 2d 1897, 1908 (Fed. Cir. 1990) (en banc), cert. denied, 500 U.S. 904 (1991). It is not enough, however, that the prior art reference discloses all the claimed elements in isolation. Rather, “[a]nticipation requires the presence in a single prior reference disclosure of each and every element of the claimed invention, *arranged as in the claim.*” *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)) (emphasis added). “The *identical invention* must be shown in as complete detail as is contained

in the ... claim.” *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989); MPEP § 2131 (emphasis added).

***b) The Reference***

*Manning* teaches a memory device which can be accessed using latched row and column addresses. (Col. 4, lines 10-28). The device may also be accessed using a high-speed burst mode of operation, wherein the address is incremented internal to the device, using transitions of the column address select (/CAS) signal, following the assertion of a single external column address. (Col. 4, lines 29-49). Switching between the burst extended data out (EDO) mode and the standard EDO mode is described. (Col. 6, lines 14-22). Switching between interleaved and linear addressing modes is mentioned. (Col. 6, lines 30-34). The possibility of applying a pipelined architecture to Manning’s invention is also mentioned. (Col. 5, lines 43-46). Operation of the pipelined architecture is said to be characterized by having a memory throughput of less than one access per cycle, such that the data coming out of the device is offset by some number of cycles equal to the pipeline length. (Col. 5, lines 46-50). However, no details of how to apply the architecture, or its operation, are given.

***c) Discussion of the Rejections***

***c.1 -- The rejection under § 112***

Claim 61 was rejected under 35 USC § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. It has also been requested that this feature be added to the drawings. Because a *prima facie* case of lack of written description has not been made, and because the requisite information has indeed been disclosed in the Application as filed, the Appellants respectfully traverse this rejection.

It is asserted in the Office Action that the limitation “while in the burst mode of operation, generating at least one subsequent internal address patterned after the initial external address while in the pipelined mode of operation” was not described in the specification. However, this element is in fact described in the Application as filed.

The Appellants have made references in other responses to the following text in the Application: pg. 27, lines 1-11; pg. 38, lines 11-15; and pg. 39, lines 9-16. The attention of the Examiner is now also directed to pg. 33, lines 13-21 and pg. 38, lines 11-15 of the Application. In these passages it is noted that some embodiments enable "using an initial externally generated address followed by one or more internally generated addresses" as well as "switching between burst access ... and ... pipelined modes of operation without ceasing." Further, "... in column-based switching, switching between burst EDO and pipelined EDO modes is accomplished on successive /CAS cycles ... this type of switching may be accomplished on either read or write cycles, e.g., from a burst EDO read cycle to a pipelined EDO read cycle, and vice-versa, or from a burst EDO write cycle to a pipelined EDO write cycle and vice-versa." Finally, as noted on pg. 27, lines 5-11, "After a first /CAS signal 114 cycle in burst mode which uses the initial external values supplied for addresses XA0 and XA1, counter 149 increments those initial values and provides new internally generated addresses A0 and A1 by supplying count 0 signal 140 and count 1 signal 141 to respective A0 and A1 locations in temporary storage 119 through MUXs 125, 124. In this manner, internal addresses may be generated based on an initial external address."

It is respectfully noted that "An application need not contain a word-for-word description of the claimed invention to satisfy the written description requirement. ... All that is needed is that the application reasonably convey the claimed subject matter." See Patent Prosecution: Practice and Procedure Before the U.S. Patent Office by Irah H. Donner, pg. 738, 2002.

Since a prima facie case of lack of written description has not been made, and because the requisite information has indeed been disclosed in the Application as filed, it is respectfully requested that the rejection under 35 USC § 112, first paragraph, be reconsidered and withdrawn.

#### **c.2 -- The rejection under § 102**

Claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64 were rejected under 35 U.S.C. § 102(e) as being anticipated by Manning. First, the Appellants do not admit that Manning is prior art and reserve the right to swear behind this reference in the future. Second, the Appellants respectfully submit that a case of anticipation under 35 U.S.C. § 102(e) has not been established because

Manning does not disclose each and every element of claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64. Therefore, the Appellants respectfully traverse this rejection under 35 USC § 102(e).

*c.2.1. Why the reference does not disclose each and every element of the claimed subject matter as arranged in the claims.*

Manning specifically fails to disclose "circuitry ... configured to switch between the pipelined mode and the burst mode" as claimed by the Appellants in claim 1. Similarly, Manning fails to disclose that the burst mode and the pipelined mode are "extended data out modes" (claims 2-4); or that the "pipelined/burst mode circuitry" includes: a "buffer for storing an (external) address", a "counter for incrementing an address", "is coupled for receiving an external address", or "multiplexed devices for providing an internally generated address" (claims 5-9).

Further, Manning does not teach "selecting between" a "burst mode ... and" a "pipelined mode", or switching between such modes (claims 33-34, 46, 59-61); much less how addresses are supplied while selecting or switching modes (claim 35), or what type of switching environment may be used in burst and pipelined modes of operation (claims 48-49). Finally, Manning does not describe a system including a microprocessor and memory "selectively operable either in a burst mode or a pipelined mode", or a storage device/memory including circuitry "switchable between burst and pipeline modes of operation" (claims 50, and 63-64).

Several assertions were made in the Office Action which attribute support to various concepts allegedly disclosed by Manning. However, a careful reading of each citation reveals that the discussion of the asserted elements is incorrect. These assertions have been made with respect to:

Claims 2, 3 - Manning does not disclose that the pipelined mode is an EDO mode of operation (the two concepts are never discussed in conjunction with each other).

Claim 9 - Manning does not disclose mode selection circuitry which includes a multiplexed device (the components referenced in the Office Action are an address counter 26 and a column address decoder 30).

Claim 34 - Manning does not disclose switching between the pipelined mode and the burst mode (Manning merely refers to the possibility of using a pipelined architecture).



Claim 35 - Manning does not disclose selecting an external address along with selecting between a burst mode and a pipelined mode (since Manning never discloses selecting between burst and pipelined modes in the same device).

Claims 48, 49 - Manning does not disclose several switching environments in conjunction with burst and pipelined modes (Manning merely refers to the possibility of using a pipelined architecture).

Two more erroneous assertions are directed toward all pending claims. First, it is not true that one must "select pipeline mode" to "work in the pipeline architecture". The assertion is erroneous because the pipelined mode does not need to be selected if a device always operates in that mode. Second, in contrast to assertions tendered by the Office, the feature of switching between pipelined and burst mode operations in the same memory are included in each of the rejected claims, since each claim is directed toward a single device, accessing a single device, accessing different locations in a single device, or a single device included in a system.

*c.2.2. Why the reference does not disclose the claimed subject matter in as complete detail as is contained in the claim.*

First, it should be noted that the Office has admitted that "Manning does not specifically disclose a mode select pin and a mode control signal for selecting between a burst and a pipeline mode of operation." in an Office Action mailed to the Appellants on July 18, 2001 (Application Ser. No. 08/984,701, Paper 19, page 7) with regard to similar subject matter. If Manning does not disclose these elements, how (specifically) does Manning support switching or selecting between burst and pipelined modes of operation, as claimed in claims 1, 33, 34, 46, 50, 59, 60, 61, 63, and 64 (and in all claims that depend from them)?

Second, the Office has failed to produce a *prima facie* case of anticipation. While the assertion is made that Manning discloses "mode circuitry to select between a burst mode and a pipelined mode", and that the circuitry is "configurable to select between [the] two modes", the Appellants' representative, after a careful study of Manning, was unable to locate any such selection circuitry, nor any aspect of such circuitry which was configurable to select between burst and pipelined modes of operation.

Finally, the Office has admitted the deficiencies of Manning in a related matter with respect to several elements claimed by the Appellants in the instant Application. The attention of the Office is directed to the following assertions made by the Appellants in the appeal of U.S. Application Serial No. 08/984,561:

“Manning Col. 6, lines 14-34 merely describe burst and "standard" (i.e., page mode - see col. 6, lines 18-19) EDO operations. Manning Col. 7, lines 43-54 speaks to switching between non-EDO and EDO page modes, a static column mode, and a burst mode. Thus, Manning never discusses the ability to select or switch between burst and pipelined modes of operation...” (emphasis added)

This language was approved by the Office in a subsequent Notice of Allowability (Paper 32) mailed to the Appellants on March 21, 2003. In this Notice, the Office states:

"The claims are allowable over the prior art of record because the claims are distinguished from the prior art of record for the reasons as set forth in the ... appeal filed on 12/27/02 and because an update of a search previously made does not detect the combined claimed elements as set forth in claims 1-23."

For example, allowed claim 72 of U.S. Application Serial No. 08/984,561 reads:

A method for switching between pipeline and burst modes of operation, comprising:

maintaining a first enabling signal in an active state, the first enabling signal being an address-strobe signal;

maintaining an external mode select signal to select a pipeline mode;

receiving a stream of addresses and cycling a second enabling signal for processing the stream of addresses; and

switching the mode of operation to a burst mode on successive cycles of the second enabling signal while maintaining the first enabling signal in the active state.

Thus, the Office has approved statements by the Appellants in a related matter to the effect that Manning simply does not teach switching or selecting between the pipelined mode and other modes of operation.

Another way of viewing this issue is to ask the question: How can a memory have a pipelined architecture (as mentioned by Manning) without inherently operating in the pipelined mode (as claimed by the Appellants)? The brief answer is that a memory, such as a burst EDO memory, may include pipelined registers that permit the rapid generation of *internal* addresses. However, *external* addresses are still received and processed in the same fashion as regular EDO memory. See, for example, the definition for “Burst Extended Data Output RAM (BEDO)”, Shuttle Inc., Frequently Asked Questions, December 14, 1999, attached hereto as Appendix II.

In memory terminology, a row of memory cells is called a page. With page-mode memory, a row address is applied to the chip and the RAS signal held active while sequential column addresses are applied and the CAS signal cycled until an entire row of memory cells are read or written. By addressing columns in this manner, all of the memory cells in a selected row can be written or read without changing the row address. Since page-mode memory requires a setup time for each column address, it was eventually replaced with fast page-mode memory.

Fast page-mode memory eliminates most of the setup time for column addresses within a page, so it is faster and consumes less power than page-mode memory. With fast page-mode memory, memory accesses for an entire page were usually fast enough to reduce wait states in processors available for use with this type of memory. However, when the processor requests data from a different page, both row and column addresses have to be changed, and the resulting delay is similar to ordinary page-mode operation. See “Fast Page Mode (FPM)”, Id.

EDO memory is similar to fast page-mode memory in that an entire page of memory can be read very quickly. The major advantage of EDO memory is that it modifies CAS timing to hold data at the chip's output pins longer. This means that the output data can be read while the CAS signal is de-asserted and set up for the next cycle, resulting in less waiting. With EDO memory, data can be read or written (within a page) as fast as the memory chip will accept new column addresses. EDO allows more overlap between column accesses and data transfers than fast page-mode memory, eliminating most of the wait and resulting in a considerable performance improvement. See “Extended Data Output RAM (EDO)”, Id.

Burst EDO memory improves EDO performance by adding **a pipeline stage** (i.e., **a pipelined architecture**) to permit reads or writes to occur in four row-address bursts. After the

initial page address is applied to a burst EDO chip, the chip typically provides three more sequential addresses (within a page). This address circuitry eliminates the time required to detect and latch externally supplied addresses. However, burst EDO memory including a pipelined architecture does not accept external addresses so as to operate in a pipelined mode (as defined by the Appellants in the Application). See "Burst Extended Data Output RAM (BEDO)", Id.

As a matter of contrast, in some embodiments of the Appellants' invention, a newburst signal from control logic is provided. The newburst signal is fed to a multiplexer for choosing which type of addressing is to occur. For one type of addressing, burst operation is provided beginning with a stored initial external address. A counter is then used to increment the initial external address. (Application, Pg. 29, lines 8-25)

In pipelined mode, address information is divided into operational times. As address information passes through the memory, it is operative in one operational area before moving onto another operational area. However, once moved, another set of address information may enter the operational area exited. Thus, by time slicing address information, accesses to a memory may overlap without conflicting. This allows for a continuous data stream of address information in the form of external addresses. Therefore, **internal addresses are not generated in pipelined mode**. Rather, addresses are provided from an external source as a stream of data. In page mode, with one enable signal held active and another enable signal cycled, an external address is received on each cycle of the cycled enable signal. For example, if /RAS is held active, and /CAS is cycled, a random or determined order of columns associated with the row address may be accessed in pipelined mode, whereas in burst mode, a predetermined pattern of columns may be accessed. (Application, Pg. 8, lines 1-13)

Thus, Manning simply does not disclose any method or device for switching between burst and pipelined modes of operation. What is discussed by Manning is not identical to the subject matter of various embodiments of the invention as required by the M.P.E.P., and the rejection is under § 102 is therefore improper. Further, an updated search has been conducted by the Examiner in the referenced related matter, and none of the art reveals the ability to switch or select between burst and pipelined modes of operation. Therefore, reconsideration and allowance of claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64 is respectfully requested.

*c.3 -- Why the claims are separately patentable:*

While the separate patentability of each claim has been discussed in the "Argument" section above, as allowed in the M.P.E.P. § 1206, the reasons are summarized here to ensure completeness and as a matter of convenience for the Board.

Independent claim 1 is directed toward an asynchronously-accessible storage device having "mode circuitry configured to switch between a burst mode and a pipelined mode" and "circuitry operable in either a burst mode or pipelined mode ... for operating the asynchronously-accessible storage device in either mode." Manning does not disclose this combination of elements, and no other independent claim (or claims depending from them) has this unique combination of elements.

To the elements of independent claim 1, dependent claim 2 adds "the burst mode and the pipelined mode are extended data out modes of operation." Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

To the elements of independent claim 1, dependent claim 3 adds "the pipelined mode is an extended data out mode." Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

To the elements of independent claim 1, dependent claim 4 adds "the burst mode is an extended data out mode." Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

To the elements of independent claim 1, dependent claim 5 adds "the pipelined ... mode circuitry includes a buffer ... for storing an address." Manning does not disclose this combination of elements, and no other claim (except claim 6) has this unique combination of elements. To the elements of dependent claim 5, dependent claim 6 adds "the pipelined ... mode circuitry includes at least one counter ... for incrementing the address." Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

To the elements of independent claim 1, dependent claim 7 adds "the pipelined ... mode circuitry is coupled for reading an external address." Manning does not disclose this combination of elements, and no other claim (except claims 8 and 9) has this unique combination of elements. To the elements of dependent claim 7, dependent claim 8 adds "the pipelined ... mode circuitry

includes a buffer ... for storing the external address." To the elements of dependent claim 7, dependent claim 9 adds "the pipelined ... mode circuitry includes multiplexed devices for providing an internally generated address to the storage device." Manning does not disclose these combinations of elements, and no other claims have these unique combinations of elements.

Independent claim 33 is directed toward a method of accessing a storage device comprising "receiving a first address", "obtaining a second address", "selecting between an asynchronously-accessible burst mode and an asynchronously-accessible pipelined mode" and "asynchronously accessing a storage element of the storage device in the selected mode of operation using the first address and the second address." Manning does not disclose this combination of elements, and no other independent claim (or claims depending from them) has this unique combination of elements.

To the elements of independent claim 33, dependent claim 34 adds "switching between the burst mode and the pipelined mode." Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

To the elements of independent claim 33, dependent claim 35 adds "the second address is an external address." Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

Independent claim 46 is directed toward a method of accessing a storage device comprising "selecting a pipelined mode of operation", "providing a new external address for every access associated with asynchronously accessing the ... device while in the pipelined mode of operation", and "switching modes to a burst mode of operation". Manning does not disclose this combination of elements, and no other independent claim (or claims depending from them) has this unique combination of elements.

To the elements of independent claim 46, dependent claim 48 adds "the burst mode operates in an environment selected from the group consisting of column-based switching, row-based switching, application based switching, and fixed access-based switching." Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

To the elements of independent claim 46, dependent claim 49 adds "the pipelined mode operates in an environment selected from the group consisting of column-based switching, row-based switching, application based switching, and fixed access-based switching". Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

Independent claim 50 is directed toward a system including "a microprocessor" and "a memory coupled to the microprocessor, the memory selectively operable either in a burst mode or a pipelined mode, wherein the memory is an asynchronous dynamic random access memory". Manning does not disclose this combination of elements, and no other independent claim (or claims depending from them) has this unique combination of elements.

Independent claim 59 is directed toward a method of accessing a storage device comprising "receiving a burst/pipeline signal", "selecting between an asynchronously-accessible burst mode and an asynchronously-accessible pipelined mode ... in response to the burst/pipeline signal", and "accessing a storage element ... in the selected mode of operation". Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

Independent claim 60 is directed toward a method of accessing a storage device comprising "receiving a burst/pipeline signal", "selecting between outputting information ... and inputting information", "selecting between an asynchronously-accessible burst mode and an asynchronously-accessible pipelined mode ... in response to the burst/pipeline signal" and "asynchronously accessing a storage element ... in the selected mode of operation". Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

Independent claim 61 is directed toward a method of accessing a storage device comprising "selecting a pipeline mode of operation", "providing a new external address for every access associated with asynchronously accessing the asynchronously-accessible memory device while in a burst mode of operation", "switching modes to the burst mode of operation", and "while in the burst mode of operation, generating at least one subsequent internal address patterned after the initial external address provided while in the pipelined mode of operation".

Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

Independent claim 63 is directed toward a storage device having "an array of memory cells" and "mode circuitry for receiving a burst/pipeline signal". Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

Independent claim 64 is directed toward a memory circuit having "an array of memory cells" and "burst/pipeline selection circuitry for determining a burst or a pipeline mode of operation". Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

c.4 -- The double patenting rejection:

Claims 59 and 60 were provisionally rejected under the judicially created doctrine of double patenting over claim 36 of co-pending Application No. 08/984,563. Claim 61 was provisionally rejected under the judicially created doctrine of double patenting over claim 59 of co-pending Application No. 08/984,561.

Co-pending U.S. Patent Application Serial No. 08/984,563 has not yet received any final indication of allowed claims. The Appellants request that the claims of the instant patent application be allowed to issue without a Terminal Disclaimer, and that the issued claims of the instant application be compared to the claims of the cited co-pending application to determine if a judicially-created non-statutory double patenting rejection is required. If so, the Appellants will submit a Terminal Disclaimer to obviate any remaining double patenting rejections upon closing prosecution on the merits for the co-pending applications, as needed, or in the alternative, upon receiving an indication of allowance for the relevant claims in the instant application.

Co-pending U.S. Patent Application Serial No. 08/984,561 has received a final indication of allowed claims. The Appellants request that claim 61 of the instant application be compared to issued claim 59 of the cited co-pending application to determine if a judicially-created non-statutory double patenting rejection is required. If so, the Appellants will submit a Terminal Disclaimer to obviate any remaining double patenting rejections upon receiving an indication of allowance for claim 61 in the instant application.



## 9. SUMMARY

It is respectfully submitted that claim 61 is indeed supported by the subject matter contained in the Application as-filed, and that a *prima facie* case of anticipation under 35 U.S.C. §102 has not been established with respect to claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64. Therefore, reconsideration and withdrawal of the rejections of claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64 is respectfully requested. Should the Board be of the opinion that a rejected claim may be allowable in amended form, an explicit statement to that effect is also requested. The Examiner is invited to telephone Appellants' attorney, Mark Muller, at (210) 308-5677, or the undersigned attorney, to facilitate prosecution of this application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

JEFFREY S. MAILLOUX ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER &  
KLUTH, P.A.

P.O. Box 2938

Minneapolis, MN 55402

(612) 349-9587

Date

13 Jan '04

By

Timothy B. Clise  
Reg. No. 40,957

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 13th day of January 2004.

Name

Tina Kohut

Signature

2.1.04

## **APPENDIX I**

### **The Claims on Appeal**

1. An asynchronously-accessible storage device comprising:  
mode circuitry configured to select between a burst mode and a pipelined mode; and  
circuitry operable in either a burst mode or a pipelined mode coupled to the mode  
selection circuitry and configured to switch between the pipelined mode and the burst mode for  
operating the asynchronously-accessible storage device in either mode.
2. The asynchronously-accessible storage device of Claim 1 wherein the burst mode and the  
pipelined mode are extended data out modes of operation.
3. The asynchronously-accessible storage device of Claim 1 wherein the pipelined mode is  
an extended data out mode.
4. The asynchronously-accessible storage device of Claim 1 wherein the burst mode is an  
extended data out mode.
5. The asynchronously-accessible storage device of Claim 1 wherein the pipelined/burst  
mode circuitry includes a buffer, the buffer for storing an address.
6. The asynchronously-accessible storage device of Claim 5 wherein the pipelined/burst  
mode circuitry includes at least one counter for incrementing the address.
7. The asynchronously-accessible storage device of Claim 1 wherein the pipelined/burst  
mode circuitry is coupled for reading an external address.
8. The asynchronously-accessible storage device of Claim 7 wherein the pipelined/burst  
mode circuitry includes a buffer for storing the external address.

9. The asynchronously-accessible storage device of Claim 7 wherein the pipelined/burst mode circuitry includes multiplexed devices for providing an internally generated address to the storage device.

33. A method for accessing a storage device, comprising:  
receiving a first address to the storage device;  
selecting between an asynchronously-accessible burst mode and an asynchronously-accessible pipelined mode of operation of the storage device;  
selecting between outputting information from the storage device and inputting information to the storage device;  
obtaining a second address to the storage device; and  
asynchronously accessing a storage element of the storage device in the selected mode of operation using the first address and the second address.

34. The method of Claim 33, further comprising switching between the burst mode and the pipelined mode.

35. The method of Claim 33, wherein the second address is an external address.

46. A method for accessing several different locations in an asynchronously-accessible memory device, comprising:

selecting a pipelined mode of operation;  
providing a new external address for every access associated with asynchronously accessing the asynchronously-accessible memory device while in the pipelined mode of operation;  
switching modes to a burst mode of operation;  
providing an initial external address associated with asynchronously accessing the asynchronously-accessible memory device in the burst mode of operation; and

generating at least one subsequent internal address patterned after the initial external address while in the burst mode of operation.

48. The method of Claim 46 wherein the burst mode operates in an environment selected from the group consisting of column-based switching, row-based switching, application based switching, and fixed access-based switching.

49. The method of Claim 46 wherein the pipelined mode operates in an environment selected from the group consisting of column-based switching, row-based switching, application based switching, and fixed access-based switching.

50. A system comprising:

- a microprocessor;

- a memory, coupled to the microprocessor, the memory selectively operable either in a burst mode or a pipelined mode, wherein the memory is an asynchronous dynamic random access memory; and

- a system clock coupled to the microprocessor.

59. A method for accessing a storage device, comprising:

- receiving a first address to the storage device;

- receiving a burst/pipeline signal;

- selecting between an asynchronously-accessible burst mode and an asynchronously-accessible pipelined mode of operation of the storage device in response to the burst/pipeline signal;

- obtaining a second address to the storage device; and

- accessing a storage element of the storage device in the selected mode of operation using the first address and the second address.

60. A method for accessing a storage device, comprising:  
receiving a first address to the storage device;  
receiving a burst/pipeline signal;  
selecting between outputting information from the storage device and inputting information to the storage device;  
selecting between an asynchronously-accessible burst mode and an asynchronously-accessible pipelined mode of operation of the storage device in response to the burst/pipeline signal;  
obtaining a second address to the storage device; and  
asynchronously accessing a storage element of the storage device in the selected mode of operation using the first address and the second address.
61. A method for accessing several different locations in an asynchronously-accessible memory device, comprising:  
selecting a pipeline mode of operation;  
providing a new external address for every access associated with asynchronously accessing the asynchronously-accessible memory device while in a burst mode of operation;  
switching modes to the burst mode of operation;  
providing an initial external address associated with asynchronously accessing the asynchronously-accessible memory device in the pipelined mode of operation; and  
while in the burst mode of operation, generating at least one subsequent internal address patterned after the initial external address provided while in the pipelined mode of operation.
63. A storage device, comprising:  
an array of memory cells;  
mode circuitry for receiving a burst/pipeline signal; and  
operation circuitry operable in a burst or a pipeline mode of operation depending upon the burst/pipeline signal, the operation circuitry switchable between burst and pipeline modes of operation.

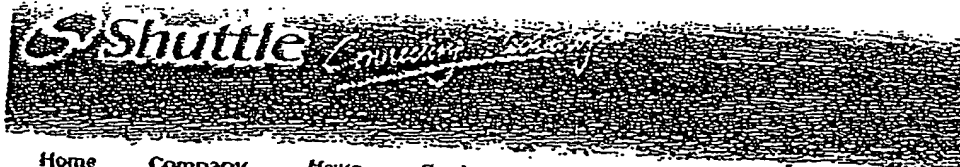
64. A memory circuit, comprising:
- an array of memory cells;
  - burst/pipeline selection circuitry for determining a burst or a pipeline mode of operation of the memory circuit; and
  - mode circuitry capable of operation in either a burst mode or a pipeline mode of operation, and switchable between burst and pipeline modes of operation.

## **APPENDIX II**

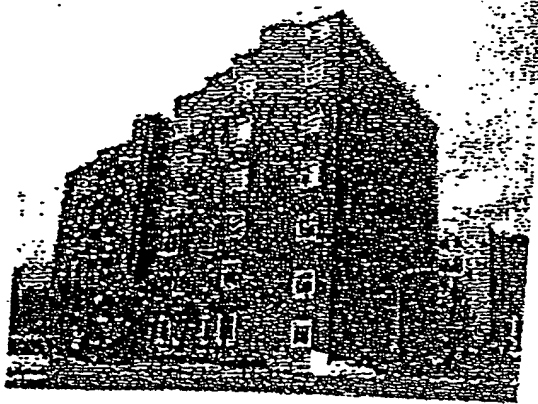
### Reference

“Burst Extended Data Output RAM (BEDO)”, Shuttle Inc., Frequently Asked Questions,  
December 14, 1999

Company



Home Company News Products Support Awards Certificates Comments Employment Where to buy



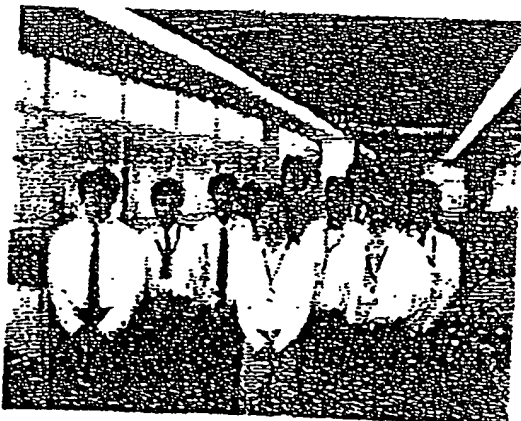
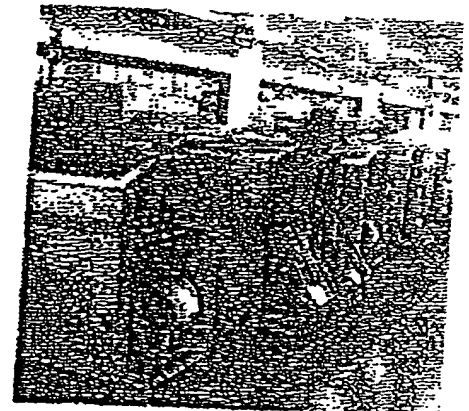
### SHUTTLE - Your Ultimate Source for PC

SHUTTLE INC., headquarters of Shuttle Group, a Taiwan based manufacturer and supplier of mainboards and add-in cards. Ever since its inception in 1983, SHUTTLE has always been recognized for its technology together with exceptional quality. Today, SHUTTLE has become one of the leading manufacturers in the world with sales revenue of US\$200 millions. Its Shuttle™ and Spacewalk™ have already reached millions of satisfied customers worldwide.

### Sales, Service and Support

SHUTTLE is a multi-national company with a strong commitment in customer service. Regional sales offices are located in the United States, Germany, Italy, Poland and Taiwan. Localization plus reliable after sales service and prompt technical support have enabled SHUTTLE to maintain a strong relationship with its customers including system integrators, VARs, OEMs, ODMs and distribution network.

In order to ensure round-the-clock service & support, SHUTTLE is accessible by E-mail, Web site and BBS.



### Research and Development

The Research and Development engineers at SHUTTLE are highly experienced and creative. For 11 years, professionals are always in pursuit of maintaining product's price per performance quality. Fully equipped with hi-end CAD tools and intensive research of up-to-date technology, professionals at SHUTTLE have provided superior products that have been proven in the market for over a decade.

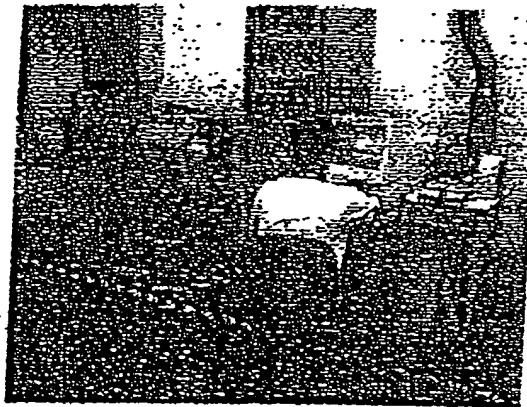
### Manufacturing

SHUTTLE is dedicated to TQM (Total Quality Management) principles. Only genuine brand name components are used in the products and strict QA/QC procedures are followed in the manufacturing process.



## Company

manufacturing process. The manufacturing facilities feature the latest in SMT equipment and manufacturing technology. ISO9001, ISO9002, and ISO14000 certified, SHUTTLE's factories yield the total production capacity of over 300K units per month. In order to keeping pace with its rapidly expanding global markets, SHUTTLE is in the process of increasing its manufacturing capacity as additional SMT lines are implemented.



## Environmental Policy

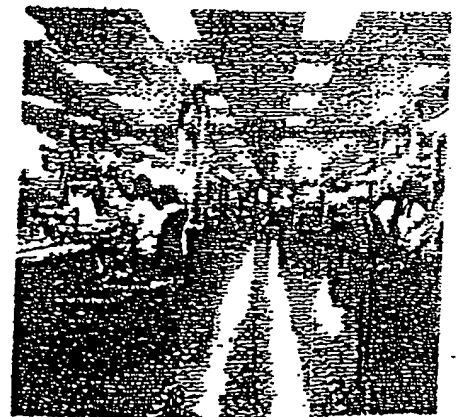
Our company is a member of the global together with the whole global enterprises to protect the green environment. We are dedicated to the protection of the environment and the prevention of environmental pollution, for the minimizing of handling of energy conservation, as well as to related legal requirements. This is to allow us to be able to have our manufactured green products eventually protect our environment.

## Our commitments:

- Strictly implement the laws and regulations
- Continuously improve the measures for preventing pollution
- Re-use the recyclable resources
- Conserve energy which shall be done by everyone
- Aspire for green products

## Commitment to Customers

SHUTTLE strongly believes in teamwork partnership with customers and remains firmly committed to delivering products with the highest quality, optimum performance and value.



## SHUTTLE Contact List

Asia

America

Germany

Company



Taiwan Head Quarters:  
Shuttle INC.  
NO. 30, Lane 76, Rei Kuang Rd.  
Nei-Hu Dist., Taipei, Taiwan  
TEL: 886-2-8792-6168  
FAX: 886-2-8792-6268



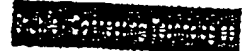
US Sales Office:  
Shuttle Computer Group INC.  
939 Radecki Court City of Industry, CA  
91748, U.S.A.  
TEL: 626-820-9000  
FAX: 626-820-5060  
<http://www.shuttleonline.com>



Germany Sales Office:  
Shuttle Computer Handels G  
Fritz-Strassmann Str. 5  
D-25337 Elmshorn, Germany  
TEL: 49-4121-476860  
FAX: 49-4121-476900

(C) 2002 Shuttle Inc.

All other brand and product names within this page are the property of their respective owners. The specification is subject to change without further notice.





## Frequently Asked Questions

[Company](#) | [Headlines](#) | [Products](#) | [Downloads](#) | [Support](#) | [Comments](#) |  
[Awards](#) | [Certificates](#) | [Employment](#) | [Search](#) | [Site Map](#) | [Home](#) |



Chapter set above: [Memory and Cache](#)

### ⚡ SIMMs and DIMMs

Chapter set below:

[SIMMs](#) (Single In Line Memory Modules)

[DIMMs](#) (Dual In Line Memory Modules)

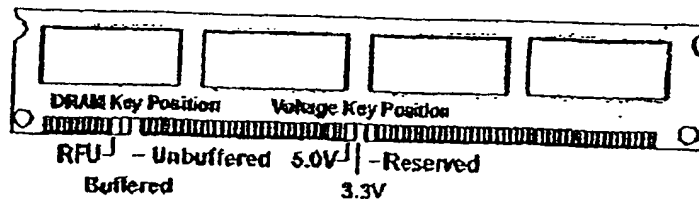
The names SIMM and DIMM only specifies the package RAM comes in, not the type! You can get each RAM type (FPM, EDO, SDRAM,...) for each module, but as far as PCs are concerned, DIMMs are at present only used for SDRAM.

#### ⚡ SIMMs (Single In Line Memory Modules)

SIMMs have 72 Pins and data path width of 32 Bit (36 Bit using Parity-Modules). On Pentium-Mainboards two SIMMs of the same kind and capacity have to be used to fill a bank. Some chipsets (for exp. SIS) allow to use only one module which results in a high performance loss.

#### ⚡ DIMMs (Dual In Line Memory Modules)

DIMMs have 168 Pins. The data path width is 64 Bit (72 Bit using Parity-Modules). For this reason you can use a single DIMM to fill a bank on a Pentium-Board. Modules must be 3.3V Unbuffered SDRAM or EDO (you can identify type as shown by the illustration above).



### ⚡ Types of memory (FPM, EDO, SDRAM, ...)

Chapter set below:

[Fast Page Mode \(FPM\)](#)

[Extended Data Output RAM \(EDO\)](#)

[Burst Extended Data Output RAM \(BEDO\)](#)

[Synchronous Dynamic RAM \(SDRAM\)](#)

#### ⚡ Fast Page Mode (FPM)

Fast Page Mode are standard memory modules. Actually VRAM or Video RAM is nothing much different, it only is so called dual ported, which means it can be accessed by the

## Shuttle Support \* SIMMs and DIMMs

RAMDAC independently of the CPU accesses via the second port, so that the RAMDAC doesn't have to wait for the CPU access to finish. FPM DRAMs for mainboards comes in two different flavors nowadays: 60ns and 70ns access time. On 66 MHz system-clock you should use 60ns modules, however, 70ns work in most cases as well. "Fast Page Mode" means that the module assumes that the next access is in the same memory area (ROW) to speed up the operation. The fastest access in CPU-Cycles is 5-3-3-3 for a data burst of 4 (Byte / Word / Dword).

### ⚡ Extended Data Output RAM (EDO)

The major difference between FPM and EDO is the timing of the CAS#-Signal and Data output using a latch. This speeds up sequential read-operations. The fastest access in CPU-Cycles is 5-2-2-2.

### ⚡ Burst Extended Data Output RAM (BEDO)

In opposition to EDO data latch on BEDO is replaced by a register (i.e. an additional latch stage is added) data will not reach the outputs as a result of the first CAS cycle. The benefit of this internal pipeline stage is that data will appear in a shorter time from the activating CAS edge in the second cycle (i.e.  $t_{cas}$  is shorter). The second difference is that BEDO devices include an internal address counter so that only the initial address in a burst of four needs to be provided externally. The fastest access in CPU-Cycles is 5-1-1-1.

### ⚡ Synchronous Dynamic RAM (SDRAM)

As the name says already, this RAM is able to handle all input and output signals synchronized to the system clock - that is something a short while ago only Static Cache RAM was able to achieve. System clock can be higher than 66Mhz. „PC/100“-modules support 100 MHz clock frequency for chipsets with this feature (e.g. Intel 440BX or VIA MVP3). The fastest access in CPU-Cycles is 5-1-1-1 (as fast as BEDO).

---

© 1999 Shuttle Inc., Last modification: 12/14/1999

All other brand and product names within this page are the property of their respective owners. Shuttle assumes no responsibility for any errors or omissions. Nor does Shuttle make any commitment to update information, with or without prior notification.

**BACK TO TOP**